REMARKS

The Official Action mailed May 1, 2002 has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time.

Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on January 24, 1997, December 8, 1997 and June 16, 2000. Applicants have not received acknowledgment of the Information Disclosure Statements filed on December 9, 1998 and December 31, 1998. It is respectfully requested that the Examiner provide an initialed copy of the Form PTO-1449 evidencing consideration.

Claims 78-157 are pending in the present application, of which claims 78, 84, 90, 96, 102, 110, 118, 126, 134, 140, 146 and 152 are independent and have been amended herewith. For the reasons set forth in detail below, these claims are believed to be in condition for allowance.

Paragraph 2 of the Official Action rejects claims 78-101, 110-115, 117-127, 129-138 and 146-157 as obvious based on the combination of U.S. Patent 4,755,865 to Wilson et al., U.S. Patent 4,772,927 to Saito et al. and U.S. Patent 4,841,348 to Shizukuishi et al. Paragraph 3 of the Official Action rejects claim 116 as being obvious based on the combination of Wilson, Saito, Shizukuishi and U.S. Patent 5,219,784 to Solheim. Paragraph 4 of the Official Action rejects claims 128 and 139 as being obvious based on the combination of Wilson, Saito and U.S. Patent 4,694,317 to Higashi et al. Paragraph 5 of the Official Action rejects claims 102-107, 109 and 140-144 as being obvious based on the combination of Wilson, Saito, Shizukuishi and U.S. Patent 4,766,471 to Ovshinsky et al. Paragraph 6 of the Official Action rejects claim 145 as being obvious based on the combination of Wilson, Saito, Shizukuishi, Ovshinsky and U.S. Patent 4,694,317 to Higashi. Finally, paragraph 7 of the Official Action rejects claim 108 as being obvious based on the combination of Wilson, Saito, Shizukuishi, Ovshinsky and U.S. Patent 5,219,784 to Solheim. Applicant respectfully traverses these rejections for the reasons that follow.

As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available

to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Furthermore, MPEP § 2112 makes clear that

> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) . . . "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) . . . . "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original) . . . ."

The Official Action asserts that Wilson teaches the entire claimed structure except for the feature of one boundary of the region (i.e. the CNO region) being located within the channel region, but that this feature is inherent in Wilson's device. The Official Action states that since Wilson's boundary between the channel region and the source/drain region is the location where dopant atoms of the source/drain region cease

to be present, the boundary is located within the channel region in which the dopant atoms are not present and that since some migration of oxygen or nitrogen occurs, the boundary would be located within the channel region as claimed.

However, Applicants respectfully assert that the Official Action's first argument is insufficient to explain that the boundary of Wilson's N or O region is necessarily located within the channel region since the boundary is clearly aligned with an edge of the gate electrode as shown in Fig. 3. In this regard, each of the independent claims has been amended herewith to further clarify that the boundary of the CNO region is not aligned with an edge of the gate electrode. Furthermore, with respect to the Official Action's second argument, since atom migration in Wilson's device is too minute, it is respectfully submitted that the teachings of Wilson do necessarily define and recognize that the boundary of the CNO region is located within the channel region. That is, it is respectfully submitted that the CNO region of Wilson would not necessarily extend into the channel region as required to maintain a rejection under the theory of inherency. Therefore, since Wilson fails to teach or suggest all of the claim limitations, it is submitted that a *prima facie* case of obviousness cannot be maintained and favorable reconsideration is requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 78, 84, 90, 96, 102, 110, 118, 126, 134, 140, 146, and 152 as follows:

78. (Amended) A semiconductor device comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary in said semiconductor layer, said region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more,

wherein one boundary of said region is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

84. (Amended) A semiconductor device comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region having a higher energy band gap than any of said source, drain, and channel regions,

wherein said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary, and one boundary of said region is located within the channel region and is not aligned with edges of the gate electrode.

90. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region formed in said semiconductor layer, said region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more,

wherein said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary, and one boundary of said region is located within the channel region and is not aligned with edges of the gate electrode.

96. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region having a higher energy band gap than any of said source, drain, and channel regions,

wherein said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary, and one boundary of said region is located within the channel region and is not aligned with edges of the gate electrode.

102. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including carbon and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including carbon is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

110. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including nitrogen and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including nitrogen is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

118. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including oxygen and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including oxygen is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

126. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region formed in the vicinity of at least one of a source-channel boundary and a drain-channel boundary in said semiconductor layer, said region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more,

wherein one boundary of said region is located within said channel region and is not aligned with edges of the gate electrode.

134. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region having a higher energy band gap than any of said source, drain, and channel regions, said region formed in the vicinity of at least one of a source-channel boundary and a drain-channel boundary in the semiconductor layer,

wherein one boundary of said region is located within said channel region and is not aligned with edges of the gate electrode.

140. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

wherein said semiconductor layer has at least one region including carbon and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including carbon is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

146. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including nitrogen and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including nitrogen is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.

152. (Amended) A semiconductor device comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including oxygen and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including oxygen is located within the channel region and is not aligned with edges of the gate electrode, and the other boundary is located within one of the source region and said drain region.